

8-Channel Source Drivers

Features and Benefits

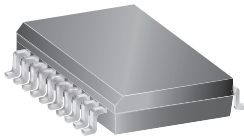
- TTL, DTL, PMOS, or CMOS compatible inputs
- 500 mA output source current capability
- Transient-protected outputs
- Output breakdown voltage to 50 V
- DIP or SOIC packaging

Packages:

Not to scale



18-pin DIP (Package A)



20-pin SOICW (package LW)
(drop-in replacement for discontinued 18-pin SOIC variants)

Description

Recommended for high-side switching applications that benefit from separate logic and load grounds, these devices encompass load supply voltages to 50 V and output currents to -500 mA. These 8-channel source drivers are useful for interfacing between low-level logic and high-current loads. Typical loads include relays, solenoids, lamps, stepper and/or servo motors, print hammers, and LEDs.

All devices may be used with 5 V logic systems—TTL, Schottky TTL, DTL, and 5 V CMOS. The device packages offered are electrically interchangeable, and will withstand a maximum output off voltage of 50 V, and operate to a minimum of 5 V. All devices in this series integrate input current limiting resistors and output transient suppression diodes, and are activated by an active high input.

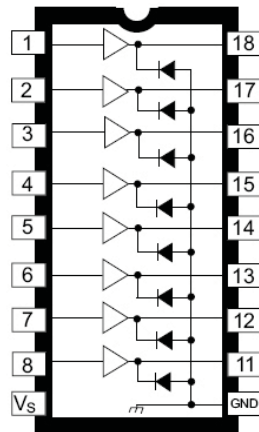
The suffix “A” indicates an 18-lead plastic dual in-line package with copper lead frame for optimum power dissipation. Under normal operating conditions, these devices will sustain 120 mA continuously for each of the eight outputs at an ambient temperature of +50°C and a supply of 15 V.

The suffix “LW” package is provided in a 20-pin wide-body SOIC package with improved thermal characteristics compared to the 18-pin SOIC version it replaces (100% pin-compatible electrically). The A2982ELW driver is available for operation over an extended temperature range, down to -40°C.

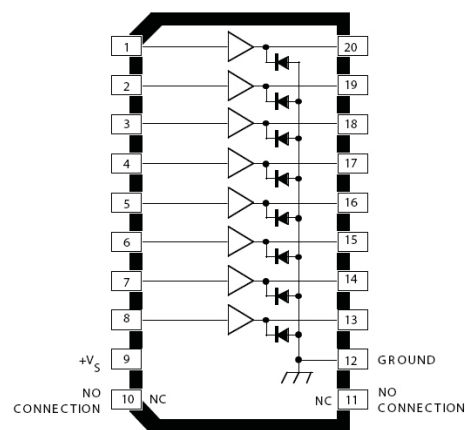
These packages are lead (Pb) free, with 100% matte-tin leadframe plating.

Simplified Block Diagrams

18-pin DIP (A Package)



20-pin SOICW (LW Package)



(NC pins, 10 and 11, not present on discontinued 18-pin LW package)

Selection Guide

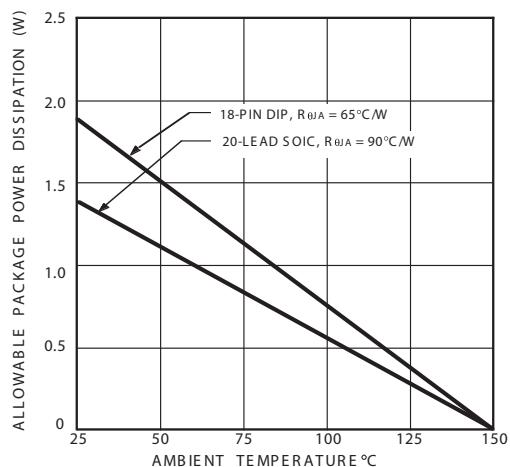
Part Number	Package	Packing	Ambient Temperature T_A (°C)
A2982ELWTR-T ¹	20-pin SOICW	1000 per reel	-40 to 85
A2982SLWTR-T	20-pin SOICW	1000 per reel	-20 to 85
UDN2981A-T ²	18-pin DIP	21 per tube	
UDN2982A-T ²	18-pin DIP	21 per tube	

¹Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change November 2, 2009. Deadline for receipt of LAST TIME BUY orders is April 30, 2010.

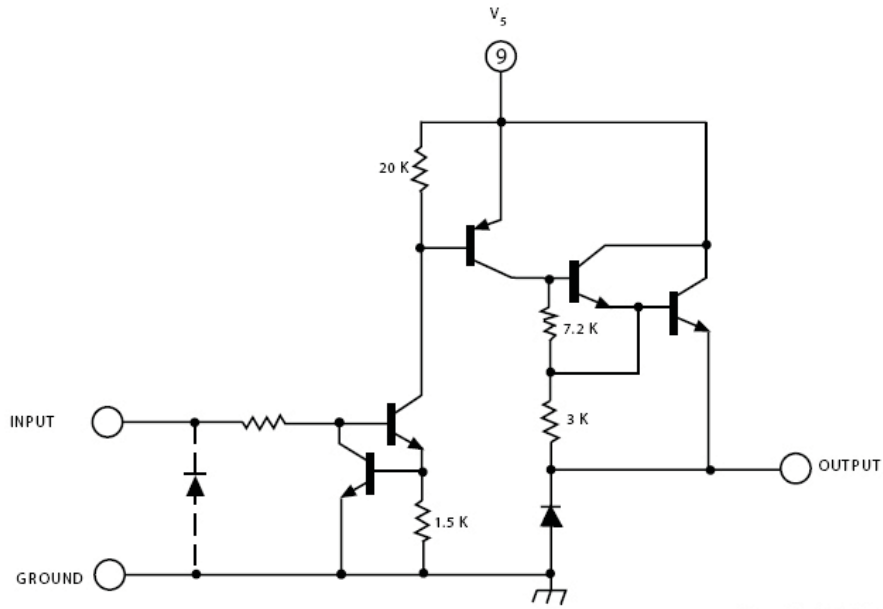
²Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change January 30, 2012. Deadline for receipt of LAST TIME BUY orders is April 27, 2012.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Output Voltage Range	V_{CE}		5 to 50	V
Input Voltage	V_{IN}	UDN2981	20	V
		A2982, UDN2982	20	V
Output Current	I_{OUT}		-500	mA
Package Power Dissipation	P_D	See graph	-	-
Operating Ambient Temperature	T_A	Range E	-40 to 85	°C
		Range S	-20 to 85	°C
Maximum Junction Temperature	$T_{J(max)}$		150	°C
Storage Temperature	T_{stg}		-55 to 150	°C



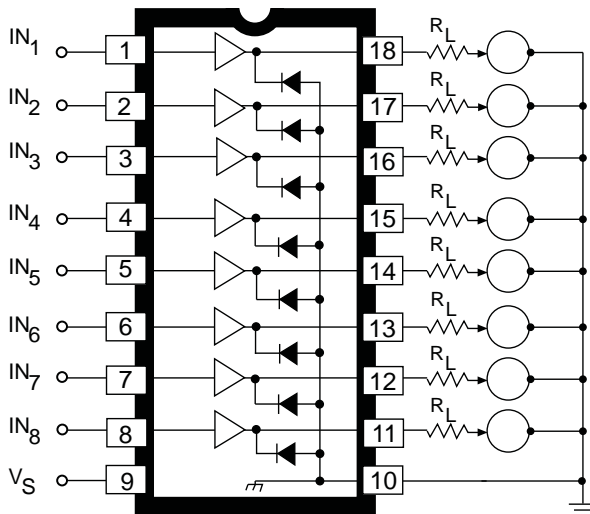
One of Eight Drivers



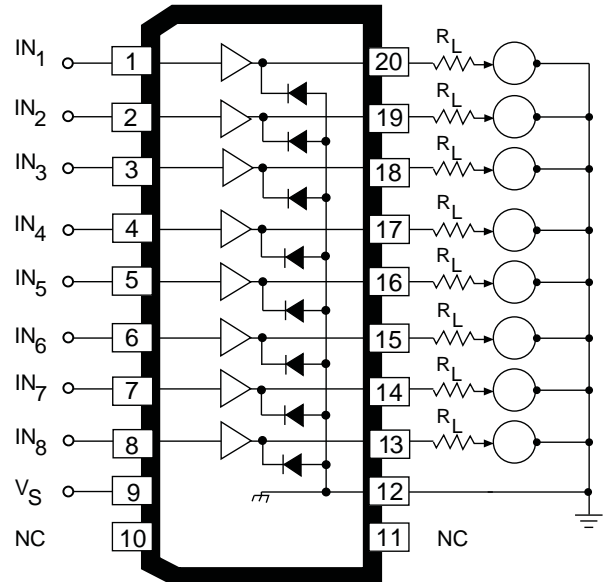
Dwg. No. A-10,242USA

Typical electroensitive
printer application

18-pin DIP (A Package)



20-pin SOICW (LW Package)



Pins 10 and 11 can float; other pins
match discontinued 18-pin SOIC: 1 to 9
same, pins 12 to 20 match pins 10 to 18

ELECTRICAL CHARACTERISTICS^{1,2} at $T_A = +25^\circ\text{C}$ (unless otherwise specified).

Characteristic	Symbol	Variant	Test Conditions	Test Fig.	Min.	Typ.	Max.	Units
Output Leakage Current ³	I_{CEX}	All	$V_{IN} = 0.4\text{ V}, V_S = 50\text{ V}$	1	—	—	20	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	All	$I_{OUT} = -45\text{ mA}$	—	35	—	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	$V_{IN} = 2.4\text{ V}, I_{OUT} = -100\text{ mA}$	2	—	1.6	1.8	V
			$V_{IN} = 2.4\text{ V}, I_{OUT} = -225\text{ mA}$	2	—	1.7	1.9	V
			$V_{IN} = 2.4\text{ V}, I_{OUT} = -350\text{ mA}$	2	—	1.8	2.0	V
Input Current	$I_{IN(ON)}$	2981	$V_{IN} = 2.4\text{ V}$	3	—	140	200	μA
			$V_{IN} = 3.85\text{ V}$	3	—	310	450	μA
		2982	$V_{IN} = 2.4\text{ V}$	3	—	140	200	μA
			$V_{IN} = 12\text{ V}$	3	—	1.25	1.93	mA
Output Source Current (Outputs Open)	I_{OUT}	2981	$V_{IN} = 2.4\text{ V}, V_{CE} = 2.0\text{ V}$	2	-350	—	—	mA
		2982	$V_{IN} = 2.4\text{ V}, V_{CE} = 2.0\text{ V}$	2	-350	—	—	mA
Supply Current Leakage Current	I_S	All	$V_{IN} = 2.4\text{ V}^*, V_S = 50\text{ V}$	4	—	—	10	mA
Clamp Diode Current	I_R	All	$V_R = 50\text{ V}, V_{IN} = 0.4\text{ V}^*$	5	—	—	50	μA
Clamp Diode Forward Voltage	V_F	All	$I_F = 350\text{ mA}$	6	—	1.5	2.0	V
Turn-On Delay	t_{ON}	All	$0.5 E_{IN}$ to $0.5 E_{OUT}, R_L = 100\Omega, V_S = 35\text{ V}$	—	—	0.3	2.0	μs
Turn-Off Delay ⁴	t_{OFF}	All	$0.5 E_{IN}$ to $0.5 E_{OUT}, R_L = 100\Omega, V_S = 35\text{ V},$ See Note	—	—	2.0	10	μs

¹Negative current is defined as coming out of (sourcing) the specified device terminal.

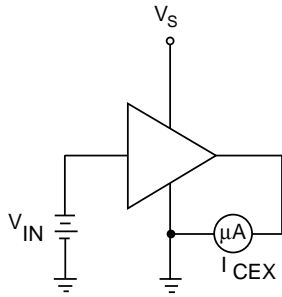
²All unused inputs must be connected to ground. Pull-down resistors (approximately 10 k Ω) are recommended for inputs that are allowed to float while power is being applied to V_S .

³All inputs simultaneously.

⁴Turn-off delay is influenced by load conditions. Systems applications well below the specified output loading may require timing considerations for some designs, i.e., multiplexed displays or when used in combination with sink drivers in a totem pole configuration.

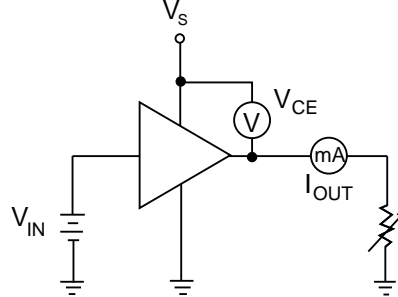
TEST FIGURES

Figure 1



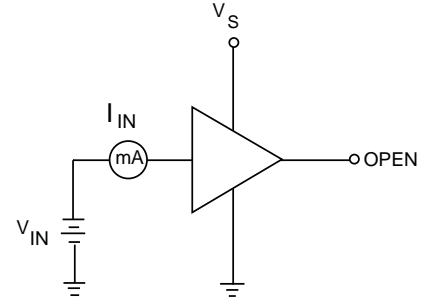
Dwg. No. A-11,083

Figure 2



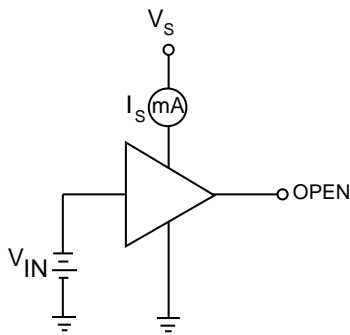
Dwg. No. A-11,084

Figure 3



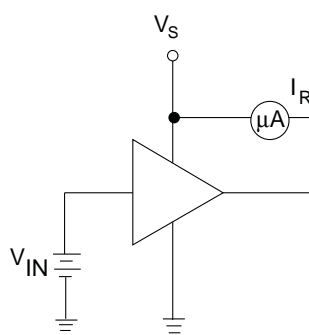
Dwg. No. A-11,085

Figure 4



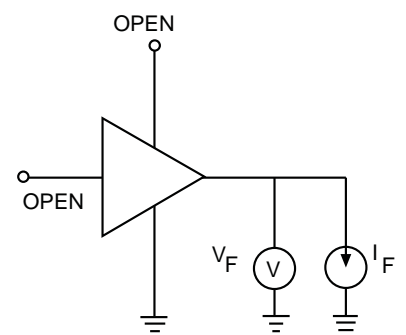
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Figure 5



Dwg. No. A-11,087

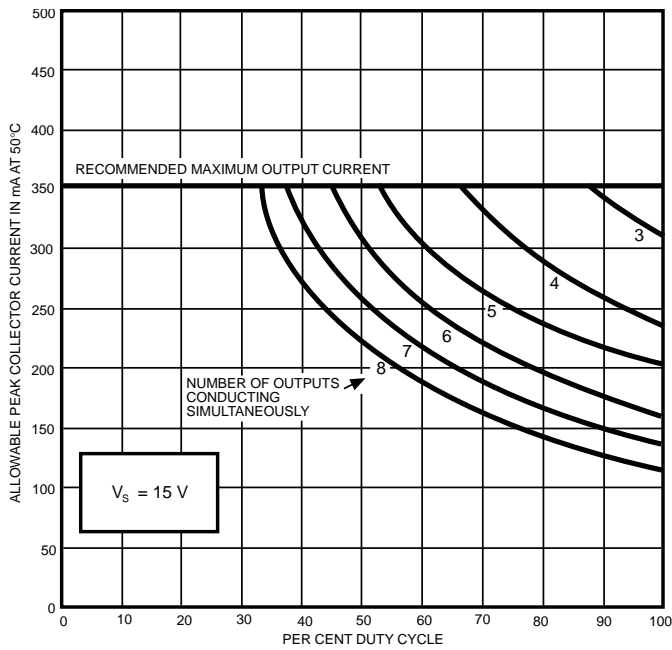
Figure 6



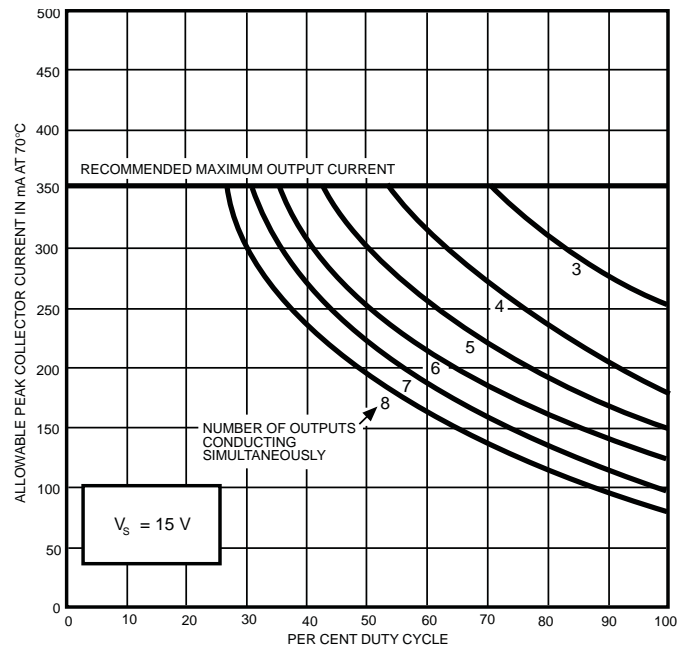
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Allowable peak collector current
as a function of duty cycle

UDN2981A and UDN2982A

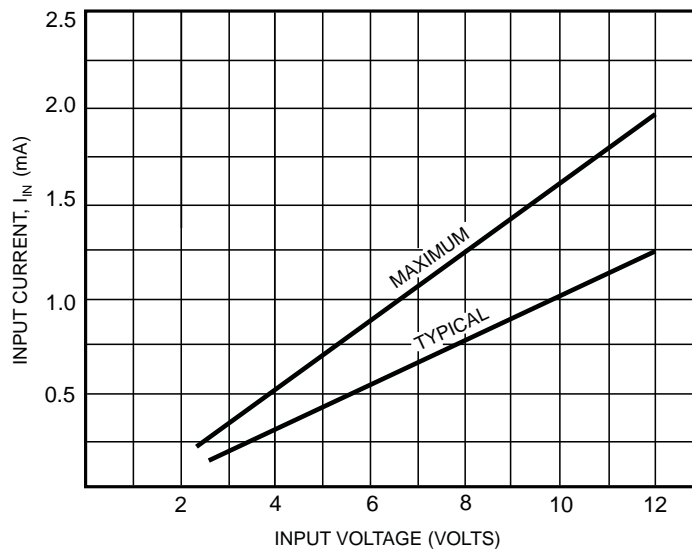


Dwg. No. A-11,107B



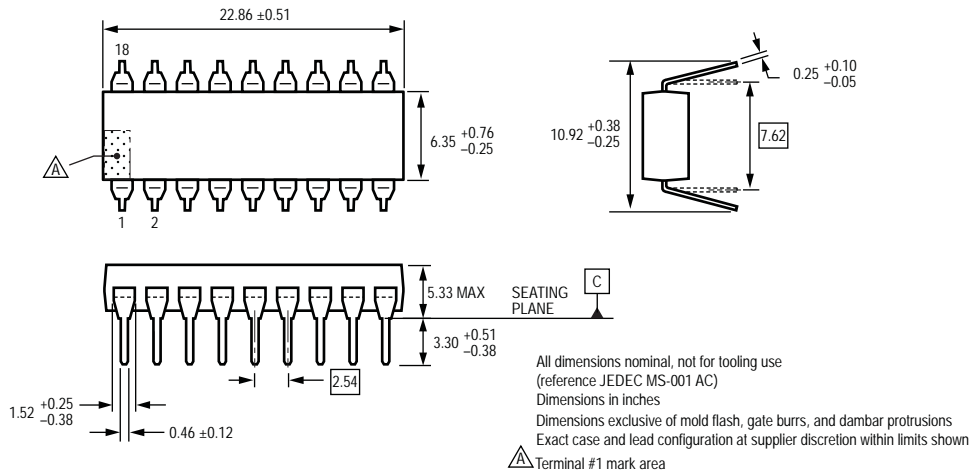
Dwg. No. A-11,108B

Input current as a function
of input voltage

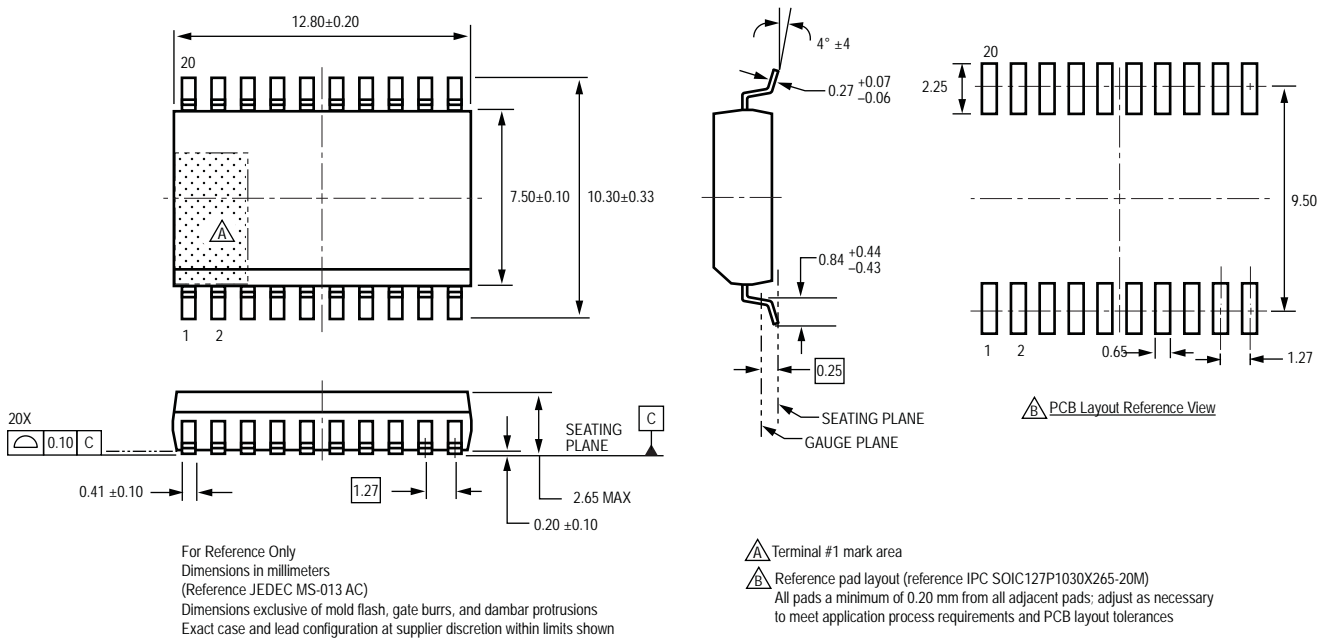


Dwg. No. A-11,115B

A Package, 18-Pin DIP



LW Package, 20-Pin SOICW



Revision History

Revision	Revision Date	Description of Revision
Rev. T	Januray 30, 2012	Update product availability

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